Testing Of FIFO Buffer of NoC Router Using Bist: Survey

S. Ram Suja
Department of Electronics and Communication Engineering, PSNA College of Engineering and Technology, Tamilnadu - 624622, India.

M. Deivakani
Department of Electronics and Communication Engineering, PSNA College of Engineering and Technology, Tamilnadu - 624622, India.

Abstract – Networks-on-Chip (NoC) is a promising solution for on-chip interconnection in SoC due to its scalability, reusability, flexibility and parallelism. It is important to identify and rectify the fault in the Network on Chip. Testing is an important process to identify and rectify the fault in Network on Chip. In testing, FIFO buffers produce high throughput gain and reduce latency. BIST (Built in Self-Test) is used for testing the routing process. BIST strategy is used for testing the NoC interconnect network and explores if the strategy is a suitable approach for the task. The intention is to use BIST to detect faults and to be able to pinpoint the location of each defect and finally use this information to reconfigure the architecture. Periodic testing of buffers prevent accumulation of faults and also allows test of each location of the buffer. The periodic testing of FIFO buffers do not have much effect on the overall throughput of the NoC, except when buffers are tested too frequently.

Index Terms – Fault tolerance, On-Chip interconnections, Built-In Self-Test.

1. INTRODUCTION

Network on Chip (NoC) is a new model to make the interconnections inside a System on Chip (SoC) system. In traditional solutions interconnections are realized using a bus structure. Bus starts to be narrow and in the worst case it begins to block traffic. In NoC technology the bus structure is changed with a network. Segments communicate with each other by sending packetized data over this network.

Networks-on-Chip (NoC) is a promising solution for on-chip interconnection in MCSoCs due to its scalability, reusability, flexibility, and parallelism. Transient and permanent faults are two different types of faults that can be able to occur in on-chip networks. Transient faults are temporary and unpredictable. They are frequently difficult to be detected and corrected. Permanent faults are caused by physical damages such as manufacturing faults and device wear-out.

These faults should be recovered or tolerated in a way that the network continues functioning. Routing techniques provide some steps of fault tolerance in NoCs. They can be categorized into deterministic and adaptive approaches. A deterministic routing algorithm uses a fixed path for each pair of nodes resulting in increased packet latency especially in congested networks. In adaptive routing algorithms, packets are not restricted to a single path when crossing over from a source to a destination router. So, they can decrease the probability of routing packets through congested areas and thus improve the performance.

In minimal adaptive routing algorithms, the shortest paths are used for transmitting messages between routers. In NoCs, faults may occur in cores (such as processing elements and memory modules), links or routers. When a core is faulty, the connected router and links can continue functioning. When a link is faulty, the approaches similar to BFT-NoC retain the connectivity by a dynamic sharing of surviving channels. Thereby, cores and routers perform functioning normally. The most severe case causes by a faulty router. In this case, not only the connected core cannot send or receive packets, but also the packets from the other cores cannot be transmitted through this router. The most common solution is to reroute packets around the faulty router or faulty region.

Considering a NoC as a network of routers and NIs, a hardware fault can occur in different places including: routers, links, and NIs. Faults in the links can be detected using a small number of test patterns. Faults in router can occur in two main parts: data-path and control-path. Data-path contains flip-flops in FIFOs, router wires, and output MUXes; control-path includes routing logics, FIFO's control part, and arbiters. When a router is in test mode, it should be tested by its neighbors. Each router contains three main test blocks: Test Pattern Generator (TPG), Test Response Analyzer (TRA), and Fault Diagnosis Module (FDM). TPG is responsible for generating test patterns and sending them to the neighbor router which is under test (RUT). TPG of the local port which is inside the router under test's NI sends test packets to the neighbors. Test response analyzer receives test patterns from the neighbor that is under test and analyzes them to detect any fault in the corresponding router and links.

2. BASICS OF ROUTER

A Router is a networking device that forward data packets between computer networks. Routers perform the traffic directing functions on the Internet. A data packet is normally forwarded from one router to another through the networks that constitute the internetwork till it reaches to its destination node. A router is connected to two or more data lines from different networks. When a data packet approaches in on one of the lines, the router reads the address information in the packet to determine the final destination. Then, using information in routing table or routing policy, it directs the packet to the resulting network on its journey.

The most familiar type of routers are home and small office routers that only permit IP packets between the home computers and the Internet. An example of a router would be the owner's cable and DSL router, which connects to the Internet over an Internet service provider (ISP).

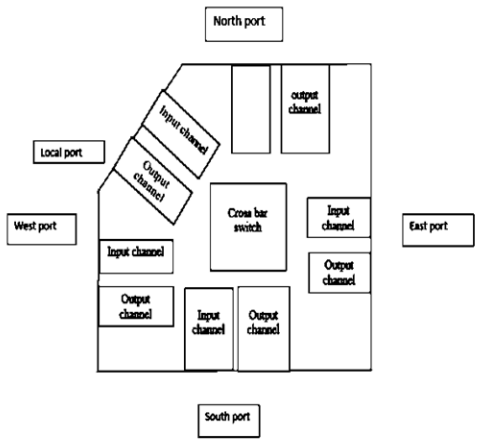

Fig 1 Router Architecture

Input Channel: There is one input channel for each port and each has its control and decoding logic. It consists of three main parts FIFO, FSM, XY logic. FIFO is used in input buffer to store the data temporarily. The size of FIFO is 8 bits and distance is of 16 bits. The first 8 bits are the header which contains coordinates of destination path. In this way the size of packet differs from 8 bits to 120 bits. The status of FIFO decides the communication can start 106 or not. If the FIFO is empty the data can be printed in it and communication can start .If FIFO is full, data can be read or can be forwarded to its destination router. Inside the router signals are used to access the FIFO. The read and write operation of FIFO is measured by FSM. FSM controls the read and write operation of FIFO according to its status. If FIFO is unoccupied and having space to store the data, FSM will generate wave signal in respect to the request coming to input channel, therefore write operation starts. If FIFO is full or not consuming space to store the data, the write operation breaks and the wave signal goes low. When the FIFO is full, FSM will send request to output channel of other port, if contribution signal is received by it then read operation jumps and continues until grant signal goes low or FIFO empties. Therefore empty position indicates the end of communication. XY logic is the deterministic logic which analyses the header of data and direct it to its destination port. The first four bits of the header organizes of destination port. In XY logic is comparator to use which compares the header of the data to the locally stored X and Y coordinate and send the packet permitting to its destination address. Let the coordinates stored in header be Hx and Hy and nearby stored coordinates be X and Y. So permitting to XY logic if Hx >X then packet will move to east port else move to west port. If Hx=X then Y coordinate is matched, If Hy >Y then packet will move to north port else move to south port, when Hy=Y then packet will move to limited port. Thus in this way XY logic will refer to the packet to the output channel of its destination p

Output Channel: Every port of the switch contains one yield channel which has its control and deciphering rationale. It additionally comprises of three sections i.e. FIFO, FSM and referee. FIFO and FSM are same as in information divert however set up of XY rationale, judge is utilized as a part of yield channel. FIFO in yield channels utilized as yield support to store the information briefly. FIFO is of size 8 bits and 16 bits. The initial 8 bits are the header which is the directions of goal switch. Along these lines size of parcel fluctuates from 8 bits to 120 bits. The status of FIFO chooses the correspondence can begin or not. In the event that the FIFO is avoid the information can be compose and correspondence can begin. On the off chance that FIFO is full, information can be perused or can be sent to its goal switch. Inside the switch the Acknowledgment signs are utilized to get to the FIFO. The read and compose operation of FIFO is measured by FSM. FSM controls the read and compose operation of FIFO as per its status. On the off chance that FIFO is unfilled or having enough space to store the information, FSM will give information in regard to the demand originating from information channel, consequently compose operation begins. In the event that FIFO is full or not having enough space to store the information, compose operation ends and the affirmation flag goes low. At the point when FIFO is full, FSM will send demand to other switch, if concede flag is gotten by it, then read operation begins and proceeds until give goes low or FIFO exhausts. Mediator is utilized as a part of yield direct set up of XY rationale in information channel. Mediator is utilized to take care of the issue of various solicitations coming at single yield port. At the point when there are more than one demand originating from one information channels to a solitary yield channel, judge chooses one of the demand and serve it. Mediator is utilized as a part of need conspire in which east has most elevated need, then west, north, south and afterward neighborhood port. As it is turning need plot, the need of port

decreases once it has been served. Accordingly this scheme expands the execution of switch as every port motivates opportunity to send its information.

In [1] proposed on the fault-oriented built-in self-test (BIST) structure of charge-pump phase-locked loop (CP-PLL) for high fault coverage and lower area overhead check solution is proposed. It employs a new structure of phase/frequency detector, a D flip-flop and some surviving blocks in the PLL as the input stimulus generator and fault feature extracted devices for testing estimate. Thus, no extra test stimulus or high-performance measured instruments are required for test. The structure is easy implementation and has a low influence on the performance of PLL. Fault simulation results indicate that the future BIST structure has high fault coverage (98.75%) and low area overhead (0.78%).

The power during testing is very greater than the functional power in [2] the BIST which affects the reliability of the chip and it is due to the less correlation between the test patterns generated by TPG. In this work a new low transition TPG is proposed and allows maximum 2 transitions between the consecutive test patterns by stepped segment activation of LFSR. The LF reduces the testing power average by 19.63% with little reduction in fault coverage. It reduce power consumption and it contain reduction in fault coverage

The fault-tolerant approaches obtainable in [3] both off-chip and on-chip networks. Regardless of all varieties, there has always been a common statement between them. Most of all known fault-tolerant methods are based on rerouting packets about faults. Rerouting might take place through non minimal paths which affect the performance significantly not only by taking long paths but also by creating hotspot around a fault. In this work, present a fault-tolerant method based on using the shortest paths. This process maintains the performance of Networks-on-Chip in the presence of errors. To avoid using non-minimal paths, the router design is slightly modified. In the new form of architecture, there is an ability to connect the parallel and orthogonal links of a faulty router such that healthy routers are kept joined to each other. Based on this design, a fault-tolerant routing algorithm is presented which is obviously much simpler than the traditional fault tolerant routing algorithms. According to this algorithm, only the shortest paths are used by packets in the presence of fault. This results keeps the performance of NoCs in faulty situations. This algorithm is highly reliable, for an example, the reliability is higher than 99.5% when there are six faulty routers in an 8×8 mesh network. It contain highly reliable.

In [4] presented the Network-on-Chip (NoC) has developed a new paradigm to add a large number of cores on a single silicon die. This work presents a complete study of Mesh-of-Tree (MoT) topology and explores its ability in communication infrastructure design for 2-D NoC. The performance of MoT based NoC have been calculated and compared with butterfly fat-tree (BFT) and two variants of mesh network for equivalent number of cores under same bisection width constraint. Simulation results in self-similar traffic show that MoT likes the advantage of having better performance than other topologies, whereas, it consumes less average packet energy than the mesh network that connects single core to each router. In area opposite, MoT occupies almost similar area like mesh network connects single core to each router. The MoT network has also been evaluated below a set of real benchmark applications and compared with the above mentioned topologies. Simulation results below application specific traffic also show the competitive potential of MoT topology in NoC design. Moreover, due to less connectivity of the routers, synthesis result shows that MoT network can be operated at higher frequency than others. Enhancing the facts into consideration, this paper establishes that like mesh and BFT, MoT can also be functional in designing NoC based systems. This work also focuses on the limitations of MoT and other tree based topologies in NoC design in current technology and counts probable solutions to make them more acceptable. It provides an efficient shortest path and it is deadlock free.

In [5] presented a new distributed on-line test tool for NoCs is proposed which scales to large-scale networks with general topologies and routing algorithms. Individual router and its links are tested using neighbor's in different phases. Only the router below test is in test mode and all other parts of the NoC are in functional mode. Experimental results show that the on-line test approach can detect stuck-at fault and short-wire faults in the routers and links. An approach to achieves 100% fault analysis for the data-path and 85% for the control paths including routing logic, FIFO's control path and the arbiter of a 5x5 router. Combination results show that the hardware overhead of our test components with TMR (Triple Module Redundancy) maintenance is 20% for covering both stuck-at and short-wire faults and 7% for covering only stuck-at faults in the 5x5 router. The average latency overhead of the 8x8 NoC is 20% and 3% in synthetic and parsec traffic benchmarks according to the model result shown in the online testing approach.

In [6] proposed a self-testable FIFO buffer, which can be embedded into larger devices. A dual port RAM and FIFO has been designed. A new test process for the macro cell has been defined aiming or detecting all possible faults in the control logic and the RAM cell. The test procedure of appropriate Built-in Self-Test architecture has been defined and independently of the size. Fault coverage and area overhead for the proposed solution are presented.

In [7] they have present two novel methods for testing the interconnect fabrics of network-on-chip (NoC) based chips. They use the concept of recursive testing, with altered degrees of parallelism in each case. The test methodologies protect the logic switching blocks and FIFO buffers that are the basic

components of NoC fabrics. The paper concludes with test time calculations for different NoC topologies and sizes.

The test data and test response delivery is attractive is reused in [8] Network on chip. However, previous techniques do not efficiently use the bandwidths of the network by delivering test packets to all cores separately, which can make high test cost and test data volume. The NoC core testing problem is formulated as a unicast-based multicast problem in order to decrease test data delivery time in the NoC. Test response data are forwarded back to the automated test equipment (ATE) through the communication channels using the opposite paths of test data delivery, which are compacted on the way from individual processor to the ATE. A new power-aware test development scheme is proposed, which is extended to cases for multiple port ATEs. Test data is more compressed before sending and a low-power test application scheme is used for the cores because power created by cores is the bottleneck of NoC test. Experimental results are presented to show the efficiency of the proposed method in reducing the NoC test cost and test data volume by comparing to the previous methods.

In [9] presented the theoretical aspects of a technique called transparent BlST for RAMs. This technique applies to any RAM test algorithm and transforms it into a clear one. The interest of the transparent test algorithms is that testing conserves the contents of the RAM. The transparent test algorithm is then used to implement a transparent BIST. This kind of BlST is very suitable for periodic testing of RAMs. The theoretical analysis presented here shows that this transparent BlST technique does not decrease the fault coverage for modeled faults, it behaves better for unmolded ones and does not rise the aliasing with respect to the initial test algorithm. Furthermore, transparent BlST involves only slightly high area overhead with respect to standard BIST. Thus, transparent BlST becomes more attractive than standard BlST then it can be used for both fabrication testing and periodic testing.

In [10] presented a BIST scheme for testing the NoC interconnect network, and investigates if the strategy is a suitable method for the task. All switches and links in the NoC are tested with BIST, running at full clock-speed, then in a functional-like mode. The BIST is carried out to BIST operation at start up, or on command. It is shown that the proposed method can be applied for different implementations of deflecting switches, and that the test time is limit to a few thousand-clock cycles with fault coverage close to 100%.

In [11] present a Variations in process parameters move the operation of integrated circuits (ICs) and pose a significant threat to be continuous scaling of transistor dimensions. Such parameter variations, however, tend to affect logic and memory circuits in changed ways. In logic, this fluctuation in device geometries might prevent them from meeting timing and power constraints and damage the parametric yield. Memories, on the other hand, experience stability failures on reason of such variations. Process limits are not exhibited as physical disparities only, transistors experience temporal device degradation as fit. Such problems are expected to further worsen with technology scaling. Resolving the problems of traditional Si-based tools by employing non-Si alternatives may not present a viable solution, the non-Si miniature devices are estimated to suffer the ill-effects of process and temporal variations as well. To circumvent these non-idealities, there is a requirement to design ICs that can adjust themselves to operate correctly under the presence of such in consistencies. In this paper, offer an overview of the process variations and time dependent degradation mechanisms. The emerging model of variation-tolerant adaptive design for both logic and memories. Interestingly, these resiliency systems transcend several design abstraction level and present circuit and micro architectural techniques to complete reliable computations in an unreliable environment.

In [12] present a Networks on Chip create the interconnection architecture of future, massively parallel multiprocessors that accumulate hundreds to thousands of processing cores on a only chip. Their integration is enabled by ongoing miniaturization of chip developed technologies following Moore's Law. It comes with the downside of the circuit elements increased exposure to failure. Research on fault tolerant Networks on Chip tries to mitigate partial failure and its effect on network act and reliability by exploiting various forms of redundancy at the suitable network layers. The article at hand analyses the failure mechanisms, fault models, diagnosis techniques, and fault tolerance methods in on-chip networks, surveys and reviews of the research of the past ten years. The most important results are summarized and open research problems and challenges are highlighted.

3. CONCLUSION

From the above discussion to perform online and periodic test of FIFO memory existing within the routers of the NoC. BIST provides high efficient testing strategy with reduced time. Periodic testing of buffers prevents accumulation of faults and also allows test for each location of the buffer. The periodic testing of FIFO buffers do not have much effect on the complete throughput of the NoC except for when buffers are tested frequently and proposed an online test technique for the routing logic that is executed simultaneously with the test of buffers and involves utilization of the unused fields of the header flits of the received data packets. The SRAM (static RAM) random access memory that keeps data bits in its memory as long as power is being supplied.

REFERENCES

[1] Cheng Huang and Meng Zhang "Built- in-Self test for fault detectionOf charge-pump phase locked loop", in 2015

[2] B.V. Bhargav Ram1, G. Harish2 and Shiva Yelampalli3 "Stepped Segment LFSR for Low Test Power BIST ", 2015 International Conference on Smart Technologies and Management for Computing,

[3] M. Ebrahimi, M. Daneshtalab, J. Plosila, and H. Tenhunen, "Minimal-path fault- tolerant approach using connection-retaining struc-ture in networks-on-chip," in Proc. 7th IEEE/ACM Int. Symp. Netw. Chip (NoCS), Apr. 2013, pp. 1–8.

[4] S. Kundu, J. Soumya, and S. Ch attopadhyay, "Design and eval-uation of mesh- of-tree based network-on-chip using virtual chan-nel router," Microprocess. Microsyst, vol. 36, no. 6, pp. 471–488, Aug. 2012.

[5] M. R. Kakoee, V. Bertacco, and L. Benini, "A distributed and topology-agnostic approach for on-line NoC testing," in Proc. 5th ACM/IEEE Int. Symp. Netw. Chip, May 2011, pp. 113–120.

[6] S. Barbagallo et al., "A parametric design of a built-in self-test FIFO embedded memory," in Proc. IEEE Int. Symp. Defect Fault Tolerance VLSI Syst., Nov. 1996, pp. 221–229.

[7] C. Grecu, P. Pande, B. Wang, A. Ivanov, and R. Saleh, "Methodologies and algorithms for testing switch-based NoC interconnects," in Proc. 20th IEEE Int. Symp. Defect Fault Tolerance VLSI Syst., Oct. 2005, pp. 238–246.

[8] D. Xiang, "A cost-effective schem e for network-on-chip router and interconnect testing," in Proc. 22nd Asian Test Symp. (ATS), Nov. 2013, pp. 207–212.

[9] M. Nicolaidis, "Theory of transparent BIST for RAMs," IEEE Trans. Comput., vol. 45, no. 10, pp. 1141–1156, Oct. 1996.

[10] K. Petersen and J. Oberg, "Toward a scalable test methodology for 2D-mesh network-on-chips," in Proc. Design, Autom., Test Eur. Conf. Exhibit., Apr. 2007, pp. 1–6.

[11] S. Ghosh and K. Roy, "Parameter variation tolerance and error resiliency: New design paradigm for the nanoscale era," Proc. IEEE, vol. 98, no. 10, pp. 1718– 1751, Oct. 2010.

[12] M. Radetzki, C. Feng, X. Zhao, and A. Jantsch, "Methods for fault tolerance in networks-on-chip," ACM Comput. Surv., vol. 46, no. 1, pp. 1–38, Jul. 2013, Art. ID 8.

[13] S.Abulhassan,M.Deivakani," Performance of analysis of a built in selftesting for low power testing", International conference on engineering trends and science humanities, 2015